REMARKS

In the office action mailed February 7, 2007 (the "Office Action"), the Examiner rejected claims 1, 2, 5, 6, 8, 9, 13, 14, 17, 18, 21, 22, 24, 26, 28, 29, 32, and 33 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,477,614 to Leddige et al. (the "Leddige patent") in view of U.S. Patent Publication No. 2004/0216018 to Cheung (the "Cheung reference") and further in view of U.S. Patent No. 6,370,601 to Baxter (the "Baxter patent"). The Examiner further rejected claims 7, 12, 23, and 34 under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent in view of the Cheung reference and Baxter patent, and further in view of U.S. Patent No. 6,782,465 to Schmidt (the "Schmidt patent"). Claims 4, 11, 20, and 31 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent, the Cheung reference, and the Baxter patent, and further in view of Jones, Throughput Expansion with FET Based Crossbar Switching (the "Jones reference"). Claims 15, 16, 25, and 27, have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leddige patent, Cheung reference and Baxter patent, and further in view of U.S. Patent Publication No. 2004/0243769 to Frame et al. (the "Frame reference").

An information disclosure statement was submitted on February 5, 2007 (the "IDS"). Applicant requests the Examiner consider the references cited in the Form PTO-1449 of the IDS and provide the attorney of record with a signed and initialed copy of the Form PTO-1449.

Claims 1, 8, 13, and 24 are patentable over the Leddige patent in view of the Cheung reference and further in view of the Baxter patent because the combined teachings of the cited references fail to teach or suggest the combination of limitations as recited by the respective claims.

For example, the combination of the references fail to teach a memory hub having a link interface, a memory device interface, and a switch as recited in claims 1, 8, 13, and 24. The Examiner relies on the Leddige patent as disclosing a "switch" that is configured to selectively couple the link interface and the memory device interface. See the Office Action at page 4. The material cited by the Examiner describes an embodiment of a memory repeater hub 720 illustrated in Figure 7. A switch, or any circuitry analogous to a switch, that selectively couples the first electrical connector 310 (shown in Figure 3 and identified by the Examiner as

being analogous to "a link interface," see the Office Action at page 4) and the second and third memory busses 321 and 322 (shown in Figure 3 and identified by the Examiner as being analogous to "a memory device interface," see id.) is not described in the cited material. The Examiner fails to identify with any greater particularity what circuit block described at column 8, lines 11-52 is analogous to a switch as recited in claims 1, 8, 13, and 24.

The circuit blocks described by the cited material have operations that are entirely different than that of the switch recited in claims 1, 8, 13, and 24. For example, the control logic 702, described at column 8, lines 36-52 is described as the "intelligence of the memory repeater hub 720" and provides appropriate control, address, and data signals to memory module devices in response to address information it receives. That is, the control logic 702 does not couple a link interface to a memory device interface, but generates signals to command operation of the memory devices. The switch, as described in the present application, is configured to simultaneously couple link interfaces and memory interfaces in a variety of arrangements. The control logic 702 does not operate in this manner, and if a "switch" were to be substituted for the control logic 702, the memory repeater hub 720 would no longer operate in accordance with its intended purpose.

Other circuit blocks described at the cited material are similarly different from the switch as recited in claims 1, 8, 13, and 24. A request handling logic 704 deserializes and separates control and address information before providing the same to the control logic 702, as well as serializes control and address information before providing the same to CMD/ADDR bus 726. See col. 8, lines 12-22. A data handling logic 746 reformats data it receives into an appropriate format to be provided to the memory devices. See col. 8, lines 23-35. These circuit blocks, as with the control logic 702, perform operations that manipulate control, address, and data signals. None of the circuit blocks operate in a manner that is related to coupling link interfaces to memory device interfaces, as recited for the switch in claims 1, 8, 13, and 24.

The Examiner has cited the Cheung reference as teaching a DMA controller located on a memory module and cited the Baxter patent as teaching an I/O register operable to store status information. Even if it is assumed for the sake of argument that the Examiner's characterization of the Cheung reference and the Baxter patent is accurate, the two references fail to make up for the deficiencies of the Leddige patent.

Given that there is not a switch described in the Leddige patent, combining the DMA controller of the Cheung reference with the Leddige patent would not provide a DMA engine coupled through a switch to the memory device interface, as recited in claims 1, 8, 13, and 24. Moreover, since the DMA controller would not be able to access the memory through a switch, it is unlikely that such modifications to the Leddige patent to include the DMA controller of the Cheung reference in the memory repeater hub would be made, as argued by the Examiner.

For the foregoing reasons, claims 1, 8, 13, and 24 are patentable over the Leddige patent in view of the Cheung reference and further in view of the Baxter patent. Claims 2 and 4-7, which depend from claim 1, claims 9, 11, and 12, which depend from claim 8, claims 14-18 and 20-23, which depend from claim 13, and claims 25-29, which depend from claim 24, are similarly patentable based on their dependency from a respective allowable base claim. Therefore, the rejection of claims 1, 2, 4-9, 11-18, and 20-29 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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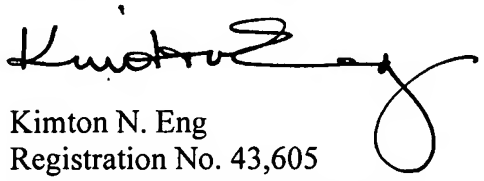

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